Claims

[c1] 1. A computer main board used within a computer, comprising:
a datapath chipset, having a peripheral configuration memory for storing an effective peripheral configuration value;
a power-supply/memory-clearing selecting circuit for switching between a power-supply status and a memory-clearing status for the peripheral configuration memory; and
a latching circuit, electrically coupled to and in between the power-supply/memory-clearing selecting circuit and the datapath chipset for providing a clearing latch signal when the power-supply status is switched to the memory-clearing status.

[c2] 2. The computer main board of claim 1, wherein the datapath chipset is a south bridge.

[c3] 3. The computer main board of claim 1, wherein the latching circuit comprises a diode and two inverting devices.

[c4] 4. The computer main board of claim 1, further comprising a basic input/output system (BIOS) that is capable of reading the clearing latch signal via the datapath chipset when the computer switches on, wherein once the clearing latch signal is set, the content of the peripheral configuration memory is cleared and the clearing latch signal is reset.

[c5] 5. The computer main board of claim 1, wherein the peripheral configuration memory comprises a volatile memory.

[c6] 6. The computer main board of claim 5, wherein the volatile memory is a complementary metal oxide semiconductor (CMOS) random access memory (RAM).

[c7] 7. A computer main board used within a computer, comprising:
a power-supply/memory-clearing selecting circuit for switching between a power-supply status and a memory-clearing status; and
a datapath chipset electrically coupled to the power-supply/memory-clearing selecting circuit, the datapath chipset comprising a peripheral configuration

memory for storing an effective peripheral configuration value and a latching circuit for providing a clearing latch signal when the power-supply status is switched to the memory-clearing status.

[c8] 8. The computer main board of claim 7, wherein the datapath chipset is a south bridge.

[c9] 9. The computer main board of claim 7, wherein the latching circuit comprises a diode and two inverting devices.

[c10] 10. The computer main board of claim 7, further comprising a basic input/output system (BIOS) that is capable of reading the clearing latch signal of the datapath chipset when the computer switches on, wherein once the clearing latch signal is set, the content of the peripheral configuration memory is cleared and the clearing latch signal is reset.

[c11] 11. The computer main board of claim 7, wherein the peripheral configuration memory comprises a volatile memory.

[c12] 12. The computer main board of claim 11, wherein the volatile memory is a complementary metal oxide semiconductor (CMOS) random access memory (RAM).

[c13] 13. A peripheral configuration memory-clearing detection circuit, used to detect a memory-clearing status that indicates the content of a peripheral configuration memory of a computer has to be cleared, the detection circuit comprising:a power-supply/memory-clearing selecting circuit for switching between a power-supply status and a memory-clearing status for the peripheral configuration memory; anda latching circuit, electrically coupled to the power-supply/memory-clearing selecting circuit for providing a clearing latch signal when the power-supply status is switched to the memory-clearing status.

[c14] 14. The detection circuit of claim 13, wherein the latching circuit comprises a diode and two inverting devices.

[c15] 15. The detection circuit of claim 13, wherein the peripheral configuration memory comprises a volatile memory.

[c16] 16. The detection circuit of claim 15, wherein the volatile memory is a complementary metal oxide semiconductor (CMOS) random access memory (RAM).

[c17] 17. A peripheral configuration memory clearing method, adapted to clear the content of a peripheral configuration memory of a computer main board, the computer main board being capable of providing a clearing latch signal that indicates whether a user has previously set a clearing of the peripheral configuration memory, the method comprising:
reading the clearing latch signal;
writing a clearing value into the peripheral configuration memory when the clearing latch signal is set; and
resetting the clearing latch signal.

[c18] 18. The method of claim 17, wherein the clearing value is "FF".

[c19] 19. The method of claim 17, wherein the peripheral configuration memory comprises a volatile memory.

[c20] 20. The method of claim 19, wherein the peripheral configuration memory is a complementary metal oxide semiconductor (CMOS) random access memory (RAM).